PATENT COOPERATION TREATY

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:
PHILIP R. WADSWORTH
5775 MOREHOUSE DRIVE
SAN DIEGO, CA 92121

PCT

NOTIFICATION OF TRANSMITTAL OF INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Rule 71.1)

Applicant's or agent's file reference 030475WO	Date of Mailing *(day/month/year)* **IMPORTANT NOTIFICATION**

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US05.06635	22 February 2005 (22.02.2005)	27 February 2004 (27.02.2004)

Applicant

QUALCOMM INCORPORATED

1. The applicant is hereby notified that this International Preliminary Examining Authority transmits herewith the international preliminary examination report and its annexes, if any, established on the international application.

2. A copy of the report and its annexes, if any, is being transmitted to the International Bureau for communication to all the elected Offices.

3. Where required by any of the elected Offices, the International Bureau will prepare an English translation of the report (but not of any annexes) and will transmit such translation to those Offices.

4. **REMINDER**

The applicant must enter the national phase before each elected Office by performing certain acts (filing translations and paying national fees) within 30 months from the priority date (or later in some Offices)(Article 39(1))(see also the reminder sent by the International Bureau with Form PCT/IB/301).

Where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary examination report. It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned.

For further details on the applicable time limits and requirements of the elected Offices, see Volume II of the PCT Applicant's Guide.

Name and mailing address of the IPEA/US	Authorized officer
Mail Stop PCT, Attn: IPEA/ US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (571)273-3201	Joseph D. Torres Telephone No. (703)746-7240

Form PCT/IPEA/416 (July 1992)

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(PCT Rule 71.1)

Date of Mailing *(day/month/year)*	23 MAR 2009

Applicant's or agent's file reference	**IMPORTANT NOTIFICATION**
030475WO	

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US05.06635	22 February 2005 (22.02.2005)	27 February 2004 (27.02.2004)

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Facsimile No. (571)273-3201	Telephone No. (703)746-7240

Form PCT/IPEA/416 (July 1992)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference 030475WO	**FOR FURTHER ACTION**	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/US05/06635	International filing date *(day/month/year)* 25 February 2005 (25.02.2005)	Priority date *(day/month/year)* 27 February 2004 (27.02.2004)

International Patent Classification (IPC) or national classification and IPC

IPC: **H03M 13/03**(2006.01);**G06F 11/00**(2006.01);**G11C 29/00**(2006.01)
USPC: 714/701,702,787,788

Applicant

QUALCOMM INCORPORATED

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 10 sheets, including this cover sheet.

   ☐ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 17 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of report with regard to novelty, inventive step and industrial applicability
   - IV ☒ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
27 September 2005 (27.09.2005)	06 March 2009 (06.03.2009)
Name and mailing address of the IPEA/US Mail Stop PCT, Attn: IPEA/ US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (571) 273-3201	Authorized officer Joseph D. Torres Telephone No. (703)-746-7240

Form PCT/IPEA/409 (cover sheet)(July 1998)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US05/06635

I. Basis of the report

1. With regard to the **elements** of the international application:*

☐ the international application as originally filed.

☒ the description:
pages 1-23 as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.

☒ the claims:
pages 24-30, as originally filed
pages NONE, as amended (together with any statement) under Article 19
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.

☒ the drawings:
pages 1-10, as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.

☐ the sequence listing part of the description:
pages NONE, as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language _____ which is:

☐ the language of a translation furnished for the purposes of international search (under Rule23.1(b)).

☐ the language of publication of the international application (under Rule 48.3(b)).

☐ the language of the translation furnished for the purposes of international preliminary examination(under Rules 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

☐ contained in the international application in printed form.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority in written form.

☐ furnished subsequently to this Authority in computer readable form.

☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. ☐ The amendments have resulted in the cancellation of:

☐ the description, pages NONE

☐ the claims, Nos. NONE

☐ the drawings, sheets/~~fig~~ NONE

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

** Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17).*
*** Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.*

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US05/06635

IV. Lack of unity of invention

1. In response to the invitation to restrict or pay additional fees the applicant has:

☐ restricted the claims.

☐ paid additional fees.

☐ paid additional fees under protest.

☐ neither restricted nor paid additional fees.

2. ☐ This Authority found that the requirement of unity of invention is not complied with and chose, according to Rule 68.1, not to invite the applicant to restrict or pay additional fees.

3. This Authority considers that the requirement of unity of invention is accordance with Rules 13.1, 13.2 and 13.3 is

☒ complied with.

☐ not complied with for the following reasons:

4. Consequently, the following parts of the international application were the subject of international preliminary examination in establishing this report:

☐ all parts.

☐ the parts relating to claims Nos. ____

V. Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. STATEMENT

Novelty (N)	Claims	2-4,7-24,26,27 and 31-34	YES
	Claims	1,5,6,25,28-30,35 and 36	NO
Inventive Step (IS)	Claims	16-19	YES
	Claims	2-4,7-15,20-24,26,27 and 31-34	NO
Industrial Applicability (IA)	Claims	1-36	YES
	Claims	NONE	NO

2. CITATIONS AND EXPLANATIONS
Please See Continuation Sheet

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

V. 2. *Citations and Explanations:*
Claims 1, 5, 6, 25, 28-30, 35 and 36 lack novelty under PCT Article 33(2) as being anticipated by Kaul; Pradman et al. (US 4063038 A, hereafter referred to as Kaul).

As per claims 1, 29, 30, 35 and 36.
Kaul teaches a mapper for receiving a first value and a second value and generating a plurality of third values (S/P block in Figure 5 of Kaul); a plurality
of memory banks, each memory bank adaptable to store one of the third values (Memory banks 1A, 1B, 2A and 2B in Figure 5 of Kaul); and a controller for
directing each of the plurality of third values to a selected one of the plurality of memory banks for simultaneous storing according to a storing pattern
(col. 9, lines 52-54 in Kaul).

As per claim 5.
Note: the S/P block generates a plurality of third channel A and channel B values and Figure 5 also teaches four memories which is twice the number of
channels (Note: a plurality of values for each channel is still a value for each channel at a particular time since it plurality of channel values at a
particular time is a numerical representation of the channel at that instance).

As per claim 6.
See output MUX in Figure 5 of Kaul.

As per claim 25.
See figure 5 in Kaul.

As per claim 28.
Demodulator 28 in Figure 1 of Kaul.

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

Claims 2-4 and 26 lack an inventive step under PCT Article 33(3) as being obvious over Kaul; Pradman et al. (US 4063038 A, hereafter referred to as Kaul).

As per claims 2-4 and 26.
Kaul substantially teaches the claimed invention described in claim 1 (as above). Note: Kaul teaches dual channel TDMA communication typically found in
many communication protocols such as QAM (one of the more commonly used dual communication protocols used for TDMA) over a bursty channel.
However Kaul does not explicitly teach the specific use of the first and second values are QAM In-phase I and Quadrature Q values.
The Examiner asserts that use of the first and second values are QAM In-phase I and Quadrature Q values are commonly used in TDMA modulation.
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kaul by including use of the first and second values are In-phase I and Quadrature Q values. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of the first and second values are In-phase I and Quadrature Q values would have provided a commonly used dual channel modulation technique for the TDMA communication system taught in Kaul.

Claim 7-10 lacks an inventive step under PCT Article 33(3) as being obvious over Kaul; Pradman et al. (US 4063038 A, hereafter referred to as Kaul) in view of Ross; Daniel P. (US 4901319 A).

As per claim 7.
Kaul substantially teaches the claimed invention described in claim 1 (as above).
However Kaul does not explicitly teach the specific use of a adaptive interleaving.
Ross, in an analogous art, teaches use of a adaptive interleaving (Abstract in Ross).
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kaul with the teachings of Ross by including use of a adaptive interleaving. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a adaptive interleaving would have provided the ability to adjust interleaving to channel conditions (Abstract in Ross).

As per claims 8 and 9.
Note: Kaul teaches dual channel TDMA communication typically found in
many communication protocols such as QAM (one of the more commonly used dual communication protocols used for TDMA) over a bursty channel.
However Kaul does not explicitly teach the specific use of the first and second values are QAM In-phase I and Quadrature Q values.
The Examiner asserts that use of the first and second values are QAM In-phase I and Quadrature Q values are commonly used in TDMA modulation.

As per claim 10.
Kaul and Ross substantially teaches the claimed invention described in claims 1 and 7 (as above). Note: Kaul teaches dual channel TDMA communication typically found in many communication protocols such as QPSK (one of the more commonly used dual communication protocols used for TDMA) over a bursty channel.

Claims 11 and 12 lack an inventive step under PCT Article 33(3) as being obvious over Kaul; Pradman et al. (US 4063038 A, hereafter referred to as Kaul) and Ross; Daniel P. (US 4901319 A) in view of Zehavi; Ephraim (US 6496543 B1).

As per claims 11 and 12.
Kaul and Ross substantially teaches the claimed invention described in claims 1 and 7 (as above).
However Kaul and Ross do not explicitly teach the specific use of 1/3 or 1/5 rate encoding.
Zehavi, in an analogous art, teaches use of 1/3 or 1/5 rate encoding (col. 9, lines 1-5 in Zehavi).
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kaul and Ross with the teachings of Zehavi by including use of 1/3 or 1/5 rate encoding. This modification would have been obvious to one of ordinary

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of 1/3 or 1/5 rate encoding would have provided a means for varying encoding rate to match channel conditions (col. 9, lines 1-5 in Zehavi).

Claim 13 lacks an inventive step under PCT Article 33(3) as being obvious over Kaul; Pradman et al. (US 4063038 A, hereafter referred to as Kaul) in view of Shiu; Da-shan et al. (US 6392572 B1, hereafter referred to as Shiu).

As per claim 13.
Kaul substantially teaches the claimed invention described in claim 1 (as above).
However Kaul does not explicitly teach the specific use of memory banks sized in accordance with one or more encoder packet sizes.
Shiu, in an analogous art, teaches use of memory banks sized in accordance with one or more encoder packet sizes (Claim 1 in Shiu).
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kaul with the teachings of Shiu by including use of memory banks sized in accordance with one or more encoder packet sizes. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of memory banks sized in accordance with one or more encoder packet sizes would have provided a means for interleaving packet data (Claim 1 in Shiu).

Claims 14, 15, 20, 21, 23 and 24 lack an inventive step under PCT Article 33(3) as being obvious over Kaul; Pradman et al. (US 4063038 A, hereafter referred to as Kaul).

As per claims 14 and 15.
Kaul substantially teaches the claimed invention described in claim 1 (as above).
However Kaul does not explicitly teach the specific use of the storing pattern comprises a plurality of cycles.
The Examiner asserts that interleaving is a method of spacing adjacent bits a given distance from each other to improve burst error correction. There are
many obvious mathematical and algorithmic ways to specify the interleave spacing without deviating from what is already known in the art.
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Kaul by including
use of the storing pattern comprises a plurality of cycles. This modification would have been obvious to one of ordinary skill in the art, at the time the
invention was made, because one of ordinary skill in the art would have recognized that use of the storing pattern comprises a plurality of cycles would
have provided a means for specifying the spacing of the interleaver (There are many obvious mathematical and algorithmic ways to specify the interleave
spacing without deviating from what is already known in the art).

As per claim 20.
Figure 5 teaches two channel for a 4-bit symbol.

As per claim 21.
Kaul substantially teaches the claimed invention described in claim 1 (as above).
However Kaul does not explicitly teach the specific use of multiplexer for implementing the S/P block in Figure 5 of Kaul.
The Examiner asserts that Multiplexers are one of the most common devices in the art for selecting and modifying data from one format to another.
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Kaul by including
use of multiplexer for implementing the S/P block in Figure 5 of Kaul. This modification would have been obvious to one of ordinary skill in the art, at
the time the invention was made, because one of ordinary skill in the art would have recognized that use of multiplexer for implementing the S/P block in
Figure 5 of Kaul would have provided one of the most common devices in the art for selecting and modifying data from one format to another as required by
the S/P block in Figure 5 of Kaul.

As per claims 23 and 24.

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

The Examiner asserts that interleaving is a method of spacing adjacent bits a given distance from each other to improve burst error correction. There are
many obvious mathematical and algorithmic ways to specify the interleave spacing without deviating from what is already known in the art.

Claim 22 lacks an inventive step under PCT Article 33(3) as being obvious over Kaul; Pradman et al. (US 4063038 A, hereafter referred to as Kaul) in view of Haoui; Amine et al. (US 5742640 A, hereafter referred to as Haoui).

As per claim 22.
Kaul substantially teaches the claimed invention described in claim 1 (as above).
However Kaul does not explicitly teach the specific use of a tri-state bus.
Haoui, in an analogous art, teaches use of a tri-state bus (MUX 106 in Figure 4 and col. 4, lines 14 19 of Haoui).
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kaul with the teachings of Haoui by including use of a tri-state bus. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a tri-state bus would have provided a means for implementing a MUX (col. 4, lines 14 19 of Haoui; Note: the S/P block in Figure 5 of Kaul is substantially a MUX).

Claim 27 lacks an inventive step under PCT Article 33(3) as being obvious over Kaul; Pradman et al. (US 4063038 A, hereafter referred to as Kaul).

As per claim 27.
Kaul substantially teaches the claimed invention described in claims 1 and 26 (as above).
However Kaul does not explicitly teach the specific use of a turbo decoder.
The Examiner asserts that of a turbo decoder is an error correction device typically used in a communication channel.
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kaul by including use of a turbo decoder. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a turbo decoder would have provided near Shannon limit error correction.

Claims 31-34 lacks an inventive step under PCT Article 33(3) as being obvious over Kaul; Pradman et al. (US 4063038 A, hereafter referred to as
Kaul).

As per claim 31.
Kaul substantially teaches the claimed invention described in claim 30 (as above).
However Kaul does not explicitly teach the specific use of an algorithm for interleaving.
The Examiner asserts that interleaving is a method of spacing adjacent bits a given distance from each other to improve burst error correction. There are
many obvious mathematical and algorithmic ways to specify the interleave spacing without deviating from what is already known in the art.
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Kaul by including use of an algorithm for interleaving. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of an algorithm for interleaving would have provided a means for specifying the spacing of the interleaver (There are many obvious mathematical and algorithmic ways to specify the interleave spacing without deviating from what is already known in the art).

As per claim 32.
The Examiner asserts that interleaving is a method of spacing adjacent bits a given distance from each other to improve burst error correction. There are
many obvious mathematical and algorithmic ways to specify the interleave spacing without deviating from what is already known in the art.

As per claim 33.
Col. 8, lines 61-68 in Kau'

As per claim 34.

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

The Examiner asserts that of a turbo decoder is an error correction device typically used in a communication channel.

Claims 16-19 meet the criteria set out in PCT Article 33(2)-(3), because the prior art does not teach or fairly suggest memory access steps such as those in claims 16-19 used in interleaving.

Claims 1-36 meet the criteria set out in PCT Article 33(4), and thus have industrial applicability because the subject matter claimed can be made or used in industry.

---------- NEW CITATIONS ----------
US 6,392,572 B1 (SHIU et al) 21 May 2002, see Claim 1.
US 4,063,038 A (KAUL et al) 13 December 1977, see Figure 5.
US 4,901,319 A (ROSS) 13 February 1990, see Abstract.
US 6,496,543 B1 (ZEHAVI) 17 December 2002, see column 9, lines 1-5.
US 5742640 A (HAOUI et al) 21 April 1998, see column 4, lines 14-19.